Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	153	(703/28).CCLS.	USPAT; USOCR	OR	OFF	2005/05/24 13:40
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L3	0	2 and over-drive	USPAT	OR	OFF	2005/05/24 13:40
L4	0	2 and (over adj voltage)	USPAT	OR	ON	2005/05/24 13:40
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L6	0	1 and (over adj current)	USPAT	OR	ON	2005/05/24 13:41
L7	0	1 and (voltage same detection)	USPAT	OR	ON	2005/05/24 13:41
L8	1	over-drive adj protection	USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/24 13:55
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L10	2099	over adj voltage adj (protection or detection)	USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2005/05/24 13:56
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L11	6	("5329471" | "5519715" | "5590354" | "5828824" | "5999008").PN. OR ("6499122").URPN.	US-PGPUB; USPAT; USOCR	OR	OFF	2005/05/24 17:20
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1 Evaluating the Effects of SEUs Affecting the Configuration Memory of an SRAM-Based FPGA

M. Bellato, P. Bernardi, D. Bortolato, A. Candelori, M. Ceschia, A. Paccagnella, M. Rebaudengo, M. Sonza Reorda, M. Violante, P. Zambolin

February 2004 **Proceedings of the conference on Design, automation and test in Europe - Volume 1**

Full text available: pdf(133.09 KB) Additional Information: full citation, abstract, index terms

This paper analyses the effects of Single Event Upsets in an SRAM-based FPGA, with special emphasis for the transient faults affecting the configuration memory. Two approaches are combined: from one side, by exploiting the available information and tools dealing with the device configuration memory, we were able to make hypothesis on the meaning of every bit in the configuration memory. From the other side, radiation testing was exploited to validate the hypothesis and to gather experimental evi ...

2 New test methods targeting non-classical faults: A novel wavelet transform based transient current analysis for fault detection and localization

Swarup Bhunia, Kaushik Roy, Jaume Segura

June 2002 **Proceedings of the 39th conference on Design automation**

Full text available: pdf(206.90 KB) Additional Information: full citation, abstract, references, citings, index terms

Transient current (IDD) based testing has been often cited and investigated as an alternative and/or supplement to quiescent current (IDDQ) testing. While the potential of IDD testing for fault detection has been established, there is no known efficient method for fault diagnosis using IDD analysis. In this paper, we present a novel integrated method for fault detection and localization using wavelet transform based IDD waveform analysis. The time-frequency resolution property of wavelet transfo ...

Keywords: fault localization, transient current (IDD), wavelet transform

3 Posters: Next-generation prototyping of sensor networks

Jan Beutel, Matthias Dyer, Martin Hinz, Lennart Meier, Matthias Ringwald

November 2004 **Proceedings of the 2nd international conference on Embedded networked sensor systems**

Full text available: pdf(382.08 KB) Additional Information: full citation, abstract, references, index terms

Large-scale deployment of sensor networks is more and more becoming an issue to researchers and industry alike. The recently revised BTnode architecture provides two wireless radios and facilitates the interconnection of heterogeneous devices. Apart from offering interesting new opportunities in using multi-frontend devices in sensor-network research, this architecture is optimally suited for deployment-support networks as introduced in the following.

4 On-Chip Multi-Channel Waveform Monitoring for Diagnostics of Mixed-Signal VLSI Circuits

Koichiro Noguchi, Makoto Nagata

March 2005 **Proceedings of the conference on Design, Automation and Test in Europe - Volume 1**

Full text available: pdf(958.85 KB) Additional Information: full citation, abstract

Multi-channel waveform monitoring technique enhances built-in test and diagnostic capability of mixed-signal VLSI circuits. An 8-channel prototype system incorporates adaptive sample time generation with a 10-bit variable step delay generator and algorithmic digitization with a 10-bit incremental reference voltage generator. The prototype in a 0.18-¿m CMOS technology demonstrated on-chip waveform acquisition at 40-ps and 200-¿V resolutions. The waveforms were as accurate as those by an off-chip ...

5 Fine-Grained Dynamic Voltage and Frequency Scaling for Precise Energy and Performance Trade-Off Based on the Ratio of Off-Chip Access to On-Chip Computation Times

Kihwan Choi, Ramakrishna Soma, Massoud Pedram

February 2004 **Proceedings of the conference on Design, automation and test in Europe - Volume 1**

Full text available: pdf(757.37 KB) Additional Information: full citation, abstract, citings, index terms

This paper presents an intra-process dynamic voltage and frequency scaling (DVFS) technique targeted toward non real-time applications running on an embedded system platform. The key idea is to make use of runtime information about the external memory access statistics in order to perform CPU voltage and frequency scaling with the goal of minimizing the energy consumption while translucently controlling the performance penalty. The proposed DVFS technique relies on dynamically-constructed regres ...

6 Efficient Test Strategy for TDMA Power Amplifiers Using Transient Current Measurements: Uses and Benefits

Ganesh Srinivasan, Soumendu Bhattacharya, Sasikumar Cherubal, Abhijit Chatterjee

February 2004 **Proceedings of the conference on Design, automation and test in Europe - Volume 1**

Full text available: pdf(207.57 KB) Additional Information: full citation, abstract, index terms

A novel algorithm for fast and accurate testing of TDMA power amplifiers in a transmitter system is presented. First, the steep cost of high frequency testers can be largely complemented by the proposed method due to its ease of implementation on low-cost testers. Secondly, TDMA power amplifiers usually have a control voltage to operate the device in various modes of operation. At each of the control voltage values, all the specifications of the power amplifier are measured to ensure the perform ...

7 Wireless application drivers for low-power systems: FSM--based power modeling of wireless protocols: the case of bluetooth

Luca Negri, Mariagiovanna Sami, David Macii, Alessandra Terranegra

August 2004 **Proceedings of the 2004 international symposium on Low power**

electronics and design

Full text available: pdf(258.49 KB) Additional Information: full citation, abstract, references, index terms

The proliferation of pervasive computing applications relying on battery--powered devices and wireless connectivity is posing great emphasis on the issue of power optimization. While node--level models and approaches have been widely discussed, a problem requiring even greater attention is that of power associated with the communication protocols. We propose a high--level modeling methodology based on Finite State Machines useful to predict the energy consumption of given communication tasks wit ...

Keywords: bluetooth, power modeling, wireless protocols

8 Moving towards more effective validation: A comparison of three verification techniques: directed testing, pseudo-random testing and property checking

Mike G. Bartley, Darren Galpin, Tim Blackmore

June 2002 **Proceedings of the 39th conference on Design automation**

Full text available: pdf(212.50 KB) Additional Information: full citation, abstract, references, index terms

This paper describes the verification of two versions of a bridge between two on-chip buses. The verification was performed just as the Infineon Technologies Design Centre in Bristol was introducing pseudo-random testing (using Specman) and property checking (using GateProp) into their verification flows and thus provides a good opportunity to compare these two techniques with the existing strategy of directed testing using VHDL bus functional models.

9 Common Reusable Verification Environment for BCA and RTL Models

Giuseppe Falconeri, Walid Naifer, Nizar Romdhane

March 2005 **Proceedings of the conference on Design, Automation and Test in Europe - Volume 3**

Full text available: pdf(142.01 KB) Additional Information: full citation, abstract

This paper deals with a common verification methodology and environment for SystemC BCA and RTL models. The aim is to save effort by avoiding the same work done twice by different people and to reuse the same environment for the two design views. Applying this methodology the verification task starts as soon as the functional specification is signed off and it runs in parallel to the models and design development. The verification environment is modeled with the aid of dedicated verification lan ...

10 Testing high-performance pipelined circuits with slow-speed testers

Muhammad Nummer, Manoj Sachdev

October 2003 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**, Volume 8 Issue 4

Full text available: pdf(213.87 KB) Additional Information: full citation, abstract, references, index terms

This article presents a methodology for testing high-performance pipelined circuits with slow-speed testers. The technique uses a clock timing circuit to control data transfer in the pipeline in test mode. The technique adds no extra hardware in the data path of the pipeline and therefore has virtually no performance penalty. A clock timing circuit capable of achieving a timing resolution of 50 ps in 0.18 µm CMOS technology is presented. The design provides the ability to test the clock timin ...

Keywords: Delay-fault testing, design for delay testability, high-performance testing

11 SystemC and SystemVerilog: Where do They Fit? Where are They Going?

Donatella Sciuto, Grant Martin, Wolfgang Rosenstiel, Stuart Swan, Frank Ghenassia, Peter Flake, Johny Srouji
February 2004 **Proceedings of the conference on Design, automation and test in Europe - Volume 1**
Full text available: pdf(93.63 KB) Additional Information: full citation, abstract, index terms

There is tremendous interest in design languages these days - and more particularly, SystemC and SystemVerilog. Sometimes the truth about design languages can be obscured by marketing and the press. This panel is meant to deepen the technical understanding of the DATE audience on the issue of design languages. It contains five technical experts - an academic expert in design languages and SystemC and SystemVerilog in particular; a language expert for each of SystemC and SystemVerilog; and a user ...

12 Multi-agent systems and social behavior: Reasoning about commitments in multiple concurrent negotiations
Thuc Duong Nguyen, Nicholas R. Jennings
March 2004 **Proceedings of the 6th international conference on Electronic commerce**
Full text available: pdf(307.16 KB) Additional Information: full citation, abstract, references

Automated negotiation by software agents is a key enabling technology for agent mediated e-commerce. To this end, this paper considers an important class of such negotiations - namely those in which an agent engages in multiple concurrent bilateral negotiations for a good or service. In particular, we consider the situation in which a buyer agent is looking for a single service provider from a number of available ones in its environment. By bargaining simultaneously with these providers and inte ...

13 Military applications: Campaign analysis: the sortie generation rate model
James W. Harris
December 2002 **Proceedings of the 34th conference on Winter simulation: exploring new frontiers**
Full text available: pdf(225.67 KB) Additional Information: full citation, abstract, references

This paper presents a sortie generation rate (SGR) model and describes how to use it as a commander's tool. The SGR model was initially developed to generate published sortie rates, but proved to be an expedient commander's tool for planning options. Previously, developing sortie rates required three models, Regional Conflict Model (RCM), Logistics Composite Model (LCOM), and Flyer. Each model required its own input data and they were located in different agencies of the Air Force. The RCM mo ...

14 MyHDL: a python-based hardware description language
Jan Decaluwe
November 2004 **Linux Journal**, Volume 2004 Issue 127
Full text available: html(20.69 KB) Additional Information: full citation, abstract

Design hardware in Python? Why not? New features of the language are making it a simple, readable choice for new hardware ideas.

15 (Special session) presentation + poster disscussion: university design contest: A bandwidth and memory efficient MPEG-4 shape encoder
Kun-Bin Lee, Nelson Yen-Chung Chang, Hao-Yun Chin, Hui-Cheng Hsu, Chein-Wei Jen
January 2004
Full text available: pdf(95.79 KB) Additional Information: full citation, abstract, references
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We have developed a shape encoder hardware for MPEG-4 video coding. On the one hand, the alpha component is compressed and therefore, the size and memory access of alpha frame memory can be reduced to 50% and 56.25% respectively. On the other hand, an efficient data transfer scheme combining the run length coding and addressing mode can reduce average data transfer time to 9.39% and accelerate the shape encoding process. The shape encoder can support MPEG-4 Main Profile at Level 4 in real-time. ...

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